High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor
Type T123-160-36

Mean on-state current		I_{TAV}	160 A	
Repetitive peak off-state voltage		V_{DRM}	3000 ÷ 3600 V	
Repetitive peak reverse voltage		V_{RRM}		
Turn-off time		t_q	400, 500 µs	
V_{DRM}, V_{RRM}, V	3000	3200	3400	3600
Voltage code	30	32	34	36
T_j, °C	-60 ÷ 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	160 200	T_c=97 °C, Double side cooled T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	251	T_c=97 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	3.2 3.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			3.5 4.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s{\cdot}10^3$	50 60	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			50 60	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3000÷3600	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3100÷3700	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.6·V_{DRM} 0.6·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	5	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	250	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 2$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60÷50	
T_j	Operating junction temperature	°C	-60÷125	
MECHANICAL				
F	Mounting force	kN	5.0÷7.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.30	$T_j=25$ °C; $I_{TM}=503$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.95	$T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	3.000		
I_L	Latching current, max	mA	500	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 1$ A/μs	
I_H	Holding current, max	mA	250	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)]	V/μs	200, 320, 500, 1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00 2.50 2.00	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	μs	3.00	$T_j=25$ °C; $V_D=1500$ V; $I_{TM}=I_{TAV}$; $di/dt=200$ A/μs; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 2$ A/μs	
t_q	Turn-off time[2)]	μs	400, 500	$dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/μs; $V_R=100$V; $V_D=0.67 \cdot V_{DRM}$	
Q_{rr} t_{rr} I_{rrM}	Total recovered charge, max Reverse recovery time, max Peak reverse recovery current, max	μC μs A	1000 20 100	$T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/μs; $V_R=100$ V	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0800	Direct current	Double side cooled
R_{thjc-A}			0.1760		Anode side cooled
R_{thjc-K}			0.1440		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0100	Direct current	
MECHANICAL					
w	Weight, typ	g	70		
D_s	Surface creepage distance	mm (inch)	7.94 (0.313)		
D_a	Air strike distance	mm (inch)	5.00 (0.197)		

PART NUMBERING GUIDE

T	123	160	36	A2	H2	N
1	2	3	4	5	6	7

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Ambient conditions: N – normal; T – tropical

NOTES

[1] Critical rate of rise of off-state voltage

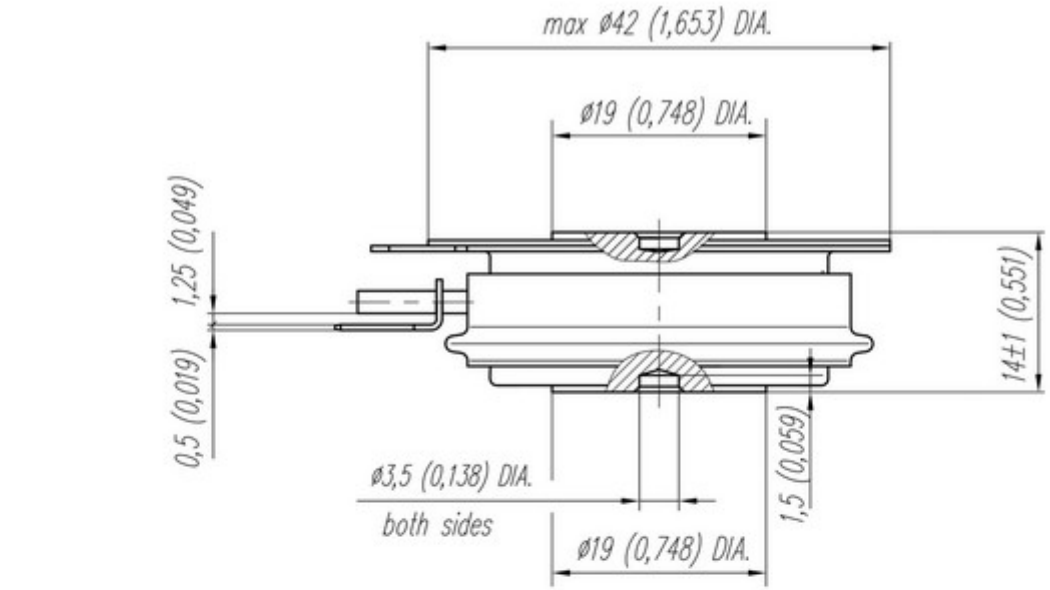
Обозначение группы	P2	K2	E2	A2
$(du_D/dt)_{crit}$, В/мкс	200	320	500	1000

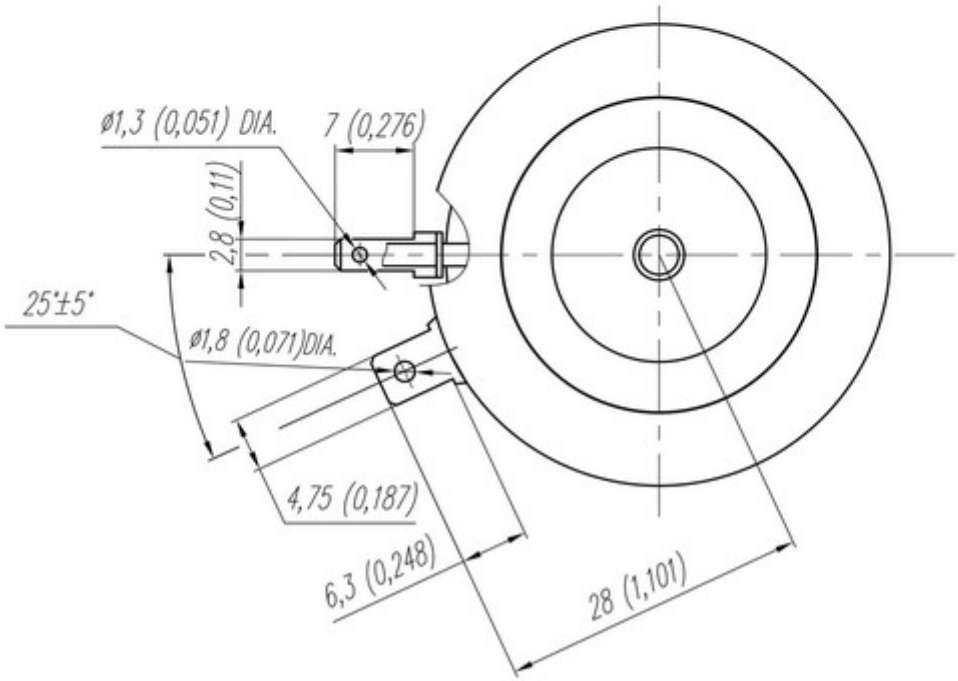
[2] Turn-off time (dv_D/dt=50 V/μs)

Обозначение группы	H2	E2
t_q, мкс	400	500

OVERALL DIMENSIONS

Package type: T.A1





All dimensions in millimeters (inches)